CLAIMS

What is claimed is:

Claim 1:

1. For use in a data processing system having an instruction processor to execute instructions included in the instruction set of the instruction processor, the instruction processor having an instruction pipeline capable of initiating simultaneous execution on a variable number of the instructions in a predetermined period of time, a system for programmably controlling the variable number of the instructions beginning execution within the instruction pipeline during the predetermined period of time, comprising:

a first storage device to receive and to store a programmable count value; and

a logic sequencer coupled to said first storage device to receive said programmable count value, and in response thereto, to generate a pipeline control signal provided to the instruction pipeline to cause the instruction pipeline to receive, and to initiate concurrent execution on, a predetermined number of the instructions in the predetermined period of time as determined by said programmable count value.

Claim 2:

2. The system of Claim 1, and further including programmable enable logic to selectively enable said logic sequencer to be responsive to said programmable count value.

Claim 3:

3. The system of Claim 2, wherein said first storage device is coupled to receive a respective programmable count value for predetermined combinations of the instructions, and wherein said programmable enable logic includes circuits to selectively enable said logic sequencer to be responsive to said respective programmable count value when a respective one of said predetermined combinations of the instructions enters the instruction pipeline.

Claim 4:

4. The system of Claim 2, wherein said first storage device is coupled to receive a respective programmable count value for predetermined combinations of the instructions only if a predetermined condition occurs within the instruction pipeline, and wherein said programmable enable logic includes circuits to selectively enable said logic sequencer to be responsive to said respective programmable count value when a respective one of said predetermined combinations of the instructions enters the instruction pipeline and only if said predetermined condition occurs within the instruction pipeline.

Claim 5:

5. The system of Claim 1, and further including scan enable logic coupled to said logic sequencer to programmably enable said logic sequencer to repeatedly generate said pipeline control signal to initiate execution of said predetermined number of the instructions during successive periods of time that are each equal to the predetermined period of time.

Claim 6:

6. The system of Claim 2, wherein said first storage device is adapted to receive, and to store, a respective first one of said programmable count values for each of first selectable ones of the instructions, and wherein said programmable enable logic includes circuits to enable said logic sequencer to receive, for any of said first selectable ones of the instructions, said respective first one of said programmable count values when said any of said first selectable ones of the instructions enters the instruction pipeline to begin execution.

Claim 7:

7. The system of Claim 6, and further comprising:

a second storage device coupled to said first storage device to store each said respective first one of said programmable count values and to provided said each respective first one of said programmable count values to said first storage device as a respective one of said first selectable ones of the instructions enters the instruction pipeline, said second storage

device further to store respective first instruction combination signals for each of said first selectable ones of the instructions;

a third storage device coupled to said logic sequencer, said third storage device adapted to store respective second instruction combination signals for each of second selectable ones of the instructions; and

a compare circuit to enable said logic sequencer to be responsive to said respective first one of said programmable count values for an executing one of the instructions N+1 where said instruction N+1 is one of said first selectable ones of the instructions and if said respective first instruction combination signals for said instruction N+1 have a predetermined relationship to said respective second instruction combination signals for one of the instructions N wherein said instruction N is one of said second selectable ones of the instructions, and is further the instruction to enter the instruction pipeline immediately before said instruction N+1.

Claim 8:

8. The system of Claim 7, wherein said third storage device further includes circuits to store microcode instructions to control execution of extended ones of the instructions, predetermined ones of said microcode instructions being associated with associated ones of said respective second instruction combination signals; and

a microsequencer coupled to said third storage device to read out a respective sequence of said microcode instructions to control execution of a respective one of said extended ones of the instructions that is being executed within the instruction pipeline, and whereby if any of said microcode instructions are said predetermined ones of said microcode instructions, to provided said associated ones of said respective second instruction combination signals to said compare circuit as said respective second instruction combination signals for said instruction N.

Claim 9:

9. The system of Claim 8, wherein said microsequencer includes conditional logic response to variable conditions within the instruction pipeline, and whereby and said respective sequence of said microcode instructions is read from said third storage device based on said variable conditions.

Claim 10:

10. The system of Claim 7, wherein said third storage device further includes circuits to store a respective second one of said programmable count values for each of said second selectable ones of the machine instructions, and further including a programmable selector coupled to said first storage device to programmably select between said respective second one of said programmable count values for said instruction N or said respective first one of said programmable count values for said instruction N+1 for use as said programmable count value.

Claim 11:

11. For use in an instruction pipeline of an instruction processor, the instruction processor to execute instructions that are part of the instruction set of the instruction processor, the instruction pipeline being adapted to initiate the execution of a variable number of instructions, up to a predetermined maximum number of instructions, within a predetermined period of time when the instruction pipeline is operating in a default mode, and whereby up to said predetermined maximum number of instructions may be executing simultaneously within the instruction pipeline, the instruction pipeline including a pipeline depth controller to generate a pipeline control signal for temporarily preventing ones of the instructions from entering the instruction pipeline, a method of utilizing the pipeline depth controller to control the number of instructions for which execution is initiated by the instruction pipeline within the predetermined period of time, comprising the steps:

providing a count to the pipeline depth controller; and

utilizing the pipeline depth controller to selectively assert the pipeline control signal to cause the instruction pipeline to initiate the execution of the number of instructions specified by said count within a period of time equal to the predetermined period of time.

Claim 12:

12. The method of Claim 11, wherein the pipeline depth controller includes a programmable enable circuit to selectively enable the generation of the pipeline control signal, and further including the step of:

programming the programmable enable circuit to enable the pipeline depth controller to repeatedly selectively assert the pipeline control signal such that the instruction pipeline initiates the execution of the number of instructions specified by said count during successive periods of time that are each equal to the predetermined period of time.

Claim 13:

13. The method of Claim 11, wherein the instruction processor includes a first memory device coupled to the pipeline depth controller, and further including the steps of:

storing within the first memory device respective first count signals for each of first predetermined ones of the instructions; and

providing said respective first count signals to the pipeline depth controller as said count when a respective one of said first predetermined ones of the instructions enters the instruction pipeline.

Claim 14:

14. The method of Claim 13, wherein the pipeline depth controller may be programmably enabled, and further including the step of:

enabling the pipeline depth controller to be responsive to said respective first count signals.

Claim 15:

15. The method of Claim 13, wherein the instruction processor includes a second memory device coupled to the pipeline depth controller, and further including the steps of:

storing within the first memory device respective first compare signals for each of said first predetermined ones of the instructions;

storing within the second memory device respective second compare signals for each of second predetermined ones of the instructions; and

comparing said respective first compare signals for an instruction N+1 that is one of said first predetermined ones of the instructions and that is executing within the instruction pipeline to said respective second compare signals for an instruction N that is one of said second predetermined ones of the instructions, and that entered the instruction pipeline for execution before said instruction N+1 entered the instruction pipeline, said comparing step performed to determine whether a predetermined relationship exists between said respective first compare signals for said instruction N+1 and said respective second compare signals for said instruction N;

and wherein said step of providing said respective first count signals to the pipeline depth controller is performed only if said predetermined relationship exists.

Claim 16:

16. The method of Claim 15, wherein the second memory device further stores microcode instructions to control the execution of ones of the instructions that are extended-mode instructions, and wherein the instruction processor includes a microsequencer to read a respective sequence of the microcode instructions from the second memory device to control execution of an instruction that is resident within the instruction pipeline, and further including the steps of:

associating predetermined ones of the microcode instructions each with a respective one of said respective second compare signals;

reading via the microsequencer the respective sequence of the microcode instructions from the second memory device for said instruction N when said instruction N is one of the extended mode instructions;

performing said comparing step using said respective second compare signals that have been associated with any said predetermined micro instruction included in said sequence of micro instructions.

Claim 17:

17. The method of Claim 16, wherein the microsequencer is responsive to variable conditions occurring within the instruction processor, and wherein said reading step is performed to select said respective sequence of the microcode instructions for said instruction N in response to said variable system conditions.

Claim 18:

18. The method of Claim 15, wherein the second memory device further stores respective second count signals for each of said second predetermined ones of the instructions, and wherein said step of providing said first respective count signals to the pipeline depth controller includes the step of selecting whether said respective second count signals will be substituted for use as said count instead of said first respective count signals.

Claim 19:

19. For use in an instruction processor having an instruction pipeline for executing multiple instructions concurrently, the instruction pipeline being capable of initiating concurrent execution for up to a predetermined maximum number of instructions within a predetermined period of time, a system for programmably controlling the number of instructions for which concurrent execution is initiated within the predetermined period of time, comprising:

storage means for receiving programmable count signals; and

sequencer means for responding to said programmable count signals, and for issuing a pipeline control signal to the instruction pipeline for controlling the entry of instructions into the instruction pipeline such that concurrent execution is initiated for the number of instructions specified by said programmable count signals within a period of time equal to the predetermined period of time.

Claim 20:

20. The system of Claim 19, wherein said storage means includes scan enable means for programmably enabling said sequencer means to issue said pipeline control signals continually such that concurrent execution is initiated for the number of instructions specified by said programmable count signals within successive periods of time each equal to the predetermined period of time.

Claim 21:

21. The system of Claim 20, and further including instruction combination means for providing respective ones of said programmable count signals to said storage means when an associated predetermined combination of the instructions has entered the instruction pipeline.

Claim 22:

22. The system of Claim 21, wherein said instruction combination means includes means for responding to variable conditions occurring within the instruction processor, and whereby said instruction combination means provides respective ones of said programmable count signals to said storage means after said associated predetermined combination of instructions has entered the instruction pipeline, and following the occurrence of a predetermined one of said variable conditions.